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Comparison of Single- and Dual-Gate FET Frequency Doublers

A. GOPINATH, SENIOR MEMBER, IEEE, ALWYN J. SEEDS, MEMBER, IEEE, AND J. B. RANKIN, MEMBER, IEEE.

Abstract—**The performance of single- and dual-gate FET frequency doublers is studied by analysis and computer simulation. The theoretical predictions are in good agreement with experimental results. It is shown that the superior performance of the dual-gate FET doubler is largely due to the higher intrinsic gain of the active device.**

I. INTRODUCTION

FET frequency doublers offer the dual attractions of conversion gain and broad-band operating capability at microwave frequencies. Experimental results for single- [1] and dual-gate [2], [3] FET doublers show that the latter offer superior conversion gain. The object of this paper is to compare the performance of single- and dual-gate doublers by means of analysis and computer simulations.

Four major sources of nonlinearity contribute to harmonic generation in both single- and dual-gate FET's:

1) The gate–source junction nonlinear capacitance;

2) The output slope conductance nonlinearity;

3) The clipping of the drain current I_d due to pinchoff, saturation, and gate–source junction forward conduction;

4) The $V_{gs}-I_d$ transfer characteristic nonlinearity.

The effect of each of these nonlinearities on harmonic generation will be discussed in turn, for each type of FET.

II. SINGLE-GATE FET DOUBLER

The nonlinear gate–source junction capacitance has, in general, a large associated series resistance, and efficient harmonic generation using the reverse biased gate–source junction is not possible [4]. The output slope conductance nonlinearity of a typical FET has been shown to be insufficient to make a significant contribution to harmonic generation [5]. When the device gate is biased close to pinchoff or forward conduction, the drain current I_d takes on a half-wave rectified form. The second harmonic component of a half-wave rectified sine wave is 7.4 dB below the corresponding fundamental frequency component, and thus, in the absence of other nonlinearities, the second-harmonic power output would be expected to be of similar magnitude (6 to 8 dB below the fundamental). With the device biased midway between pinchoff and forward conduction, the $V_{gs}-I_d$ characteristic, of the quadratic form $(1-(V_{gs}/V_p))^2$ where V_p is the pinchoff voltage, contributes a maximum second harmonic component level of 12 dB below the corresponding fundamental component at the output. Thus, frequency doubler conversion gain is at best about 6 dB below the corresponding fundamental frequency gain for gate biases close to V_p and 0 V, and somewhat less for biases between these limits. High drive levels cause symmetrical clipping of the I_d waveform due to both pinchoff and gate forward conduction, leading to reduced doubler conversion gain. These simple analytical considerations are supported by results from a large signal computer simulation based on a circuit model for the FET [5]. Fig. 1 compares simulation and experimental results for the dependence of doubler output on gate bias voltage. The experimental results were obtained for a commercial C-band medium power device (MSC 88001) in a test arrangement similar to one described previously [1], the input frequency being 4 GHz.

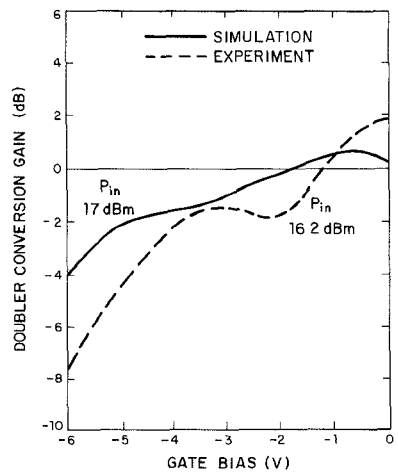

Fig. 1. Comparison of experimental and computer simulation results for a single-gate FET (MSC 88001) frequency doubler. $V_{ds}=5$ V, input frequency $f_{in}=4$ GHz.

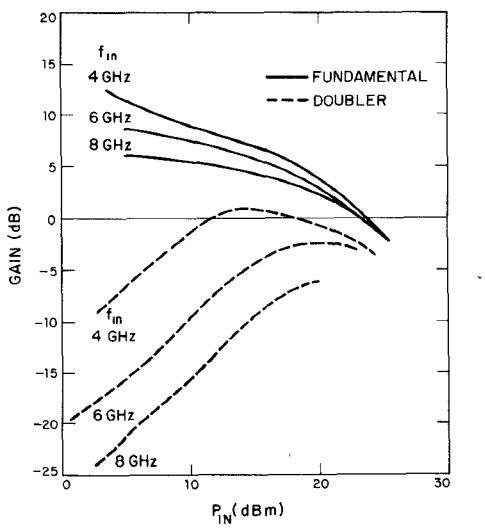

Fig. 2 Computed variation in fundamental and doubler conversion gain with frequency and drive level for a single-gate FET (MSC 88001) $V_{ds}=5$ V, $V_{gs}=0$ V.

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A. Gopinath was with Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA. 02173. He is presently with the Department of Electronics, Chelsea College, Pulton Place, London, SW6 5 PR, England.

A. J. Seeds and J B Rankin are with Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173

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The simulation results are seen to be in good agreement with measured values.

The fundamental gain of the FET falls with frequency at 6 dB per octave, and therefore a similar fall in frequency doubler conversion gain (the ratio of second harmonic output power to fundamental input power) of the FET is expected. However, parasitics and transit time effects may increase the rate of fall off. Thus the maximum value of doubler conversion gain is expected to become negative above the frequency at which the device fundamental gain falls below about 6 dB. These predictions are confirmed by Fig. 2, which shows the computed variation in fundamental and doubler conversion gain with frequency and drive level, for the FET modeled earlier.

III. Dual-Gate FET Doubler

The dual-gate FET can be modeled as two single-gate FET's in series; a grounded-source device associated with gate 1, which is adjacent to the source, and a grounded-gate device associated with gate 2, which is adjacent to the drain. However, the behavior of this structure as a doubler is more readily discerned by treating the FET as a three-terminal device, with the second gate appropriately terminated. The $I_d - V_{ds}$ characteristics of this device are similar in form to those of the single-gate FET but with the second gate bias determining the maximum saturated current. A suitable load line construction then provides a guide to the doubler behavior.

The two major sources of nonlinearity in the single-gate FET, the I_d clipping and the $V_{gs} - I_d$ transfer nonlinearity, may be accounted for in the dual-gate device on this basis. Using similar arguments to the single-gate FET, the dual-gate doubler conversion gain is about 6 to 8 dB below the corresponding input frequency fundamental gain when gate 1 is biased close to saturation and/or forward conduction, or to pinchoff, and about 12 dB lower than the fundamental gain when biased midway between pinchoff and forward conduction. As in the single-gate FET, the input gate junction is inefficient as a varactor harmonic generator, and the output slope conductance nonlinearity also does not generate significant second harmonic power. Thus the mechanisms determining the performance of the dual-gate FET doubler are similar to those for the single-gate doubler.

However, since the dual-gate FET has a small signal gain which is typically 6 dB higher than that for a comparable single-gate device, the dual-gate FET doubler conversion gain is increased by a corresponding amount. This increased gain can be seen in Fig. 3, which shows large signal simulation results for a dual-gate FET, comprising two of the single-gate devices modeled previously connected in series. The series connection of FET's gives a lower power handling capability for the dual-gate device than for the single-gate FET with equal V_{ds}. Consequently, fundamental and doubler conversion gains peak at lower values of input power. As predicted, the maximum value of dual-gate doubler conversion gain is about 6 dB less than the fundamental gain, the difference decreasing at higher input powers, with the onset of saturation. Such behavior is also shown by the single-gate device (see Fig. 2). Comparison with Fig. 2 shows that the maximum values of doubler conversion gain are 6 to 8 dB higher than those for the single-gate FET, in agreement with earlier predictions. The fundamental and doubler conversion gains fall by about 9 dB as the input frequency is increased from 4 to 8 GHz. Experimental results of Chen *et al.* [2] show similar trends to those of Fig. 3.

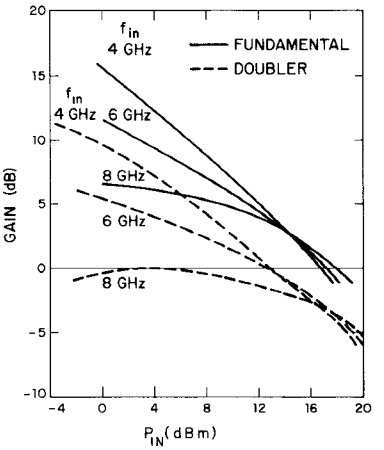

Fig 3 Computed variation in fundamental and doubler conversion gain with frequency and drive level for dual-gate FET $V_{ds} = 5$ V, $V_{g1s} = -1.5$ V, $V_{g2s} = 2$ V.

Conclusions

The paper has shown that the observed performance characteristics of single-and dual-gate FET frequency doublers are adequately described on the basis of simple analytical considerations. The apparent superior performance of the dual-gate FET doubler is found to be largely a result of the higher intrinsic device gain rather than of any increased nonlinearity.

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Quasi-Static Characteristics of Coplanar Waveguide on a Sapphire Substrate with Its Optical Axis Inclined

TOSHIHIDE KITAZAWA AND YOSHIO HAYASHI

Abstract **— A variational expression is presented for the line capacitance of a coplanar waveguide on a single-crystal sapphire substrate with a tilted optical axis. Numerical results are obtained by means of the Ritz procedure.**

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The authors are with the Department of Electronic Engineering, Kitami Institute of Technology, Kitami (090), Japan

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